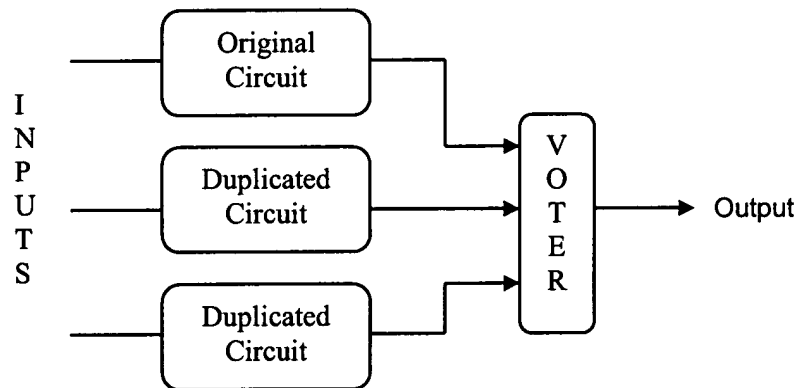




Fig. 1 Prior Art

1A



1B

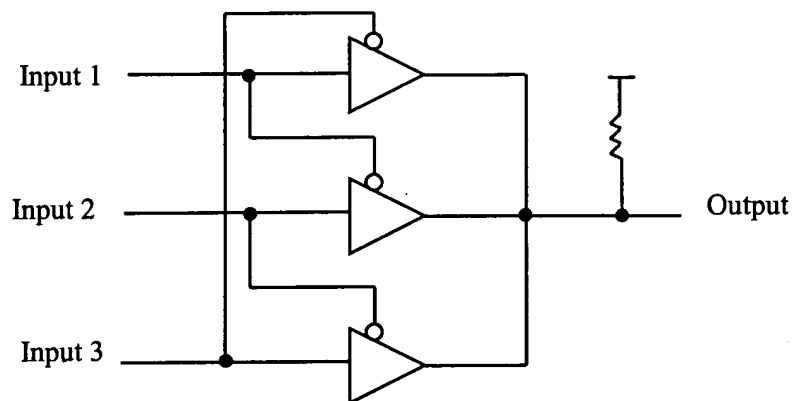


Fig. 2

Gate Type	P_{out}
AND	$\prod_i P_i$
NAND	$1 - \prod_i P_i$
OR	$\sum_i P_i - \prod_i P_i$
NOR	$1 - (\sum_i P_i - \prod_i P_i)$
XOR	$\sum_{i,j} P(i)(1-P(j))$
XNOR	$1 - (\sum_{i,j} P(i)(1-P(j)))$

Fig. 3

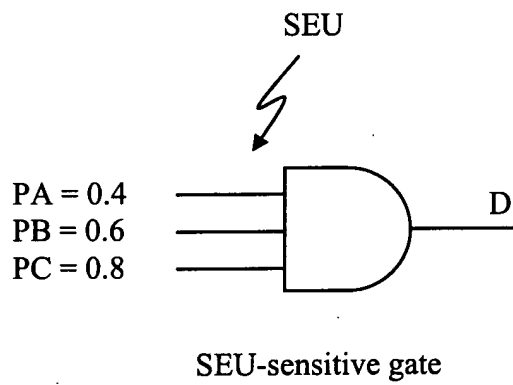
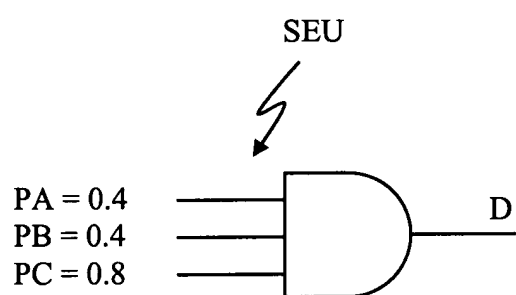


Fig. 4



SEU-insensitive gate

Fig. 5

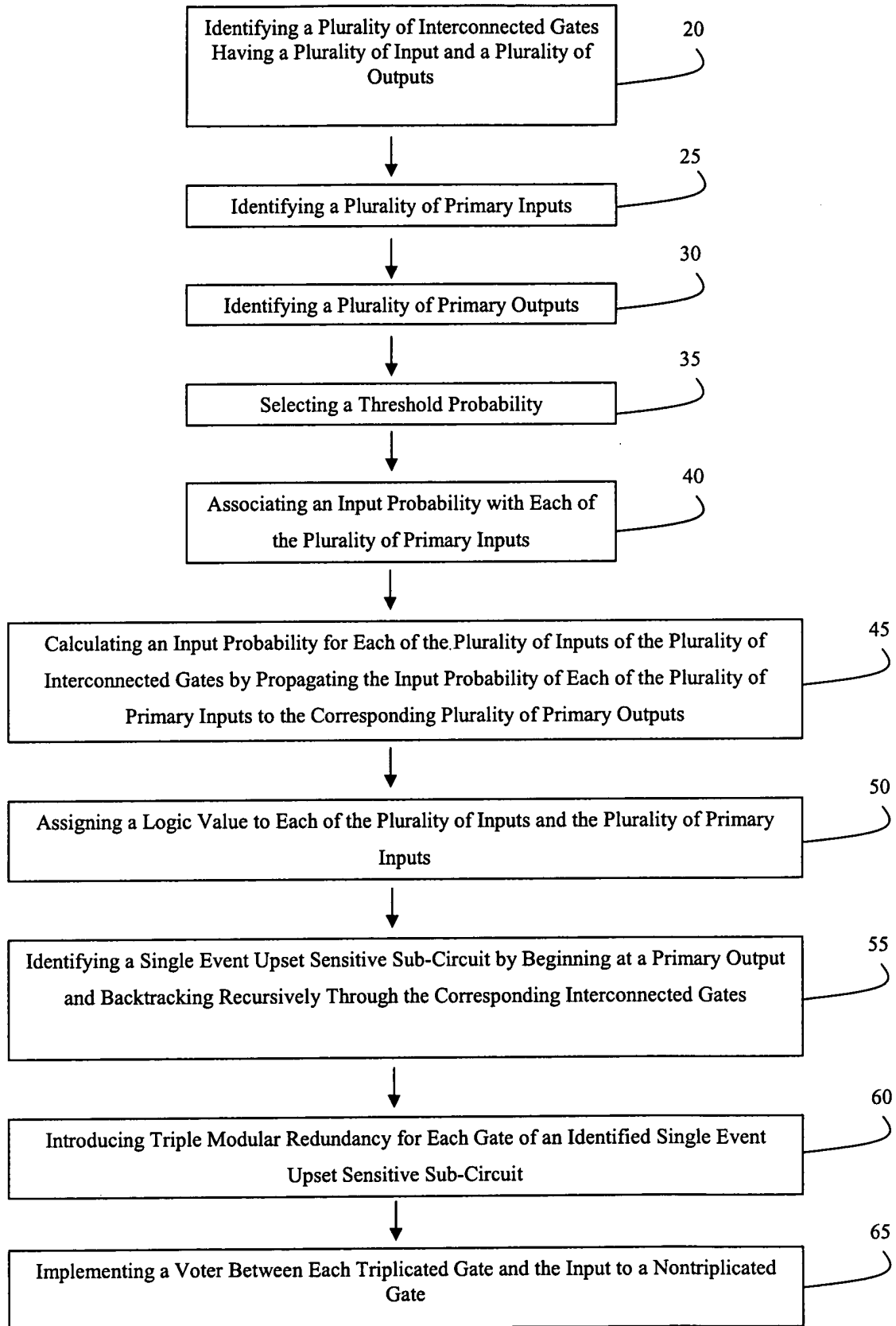
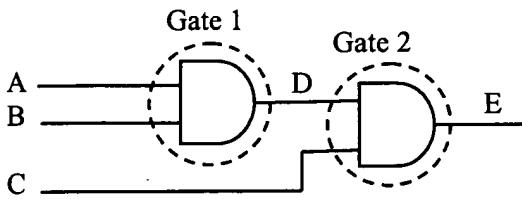
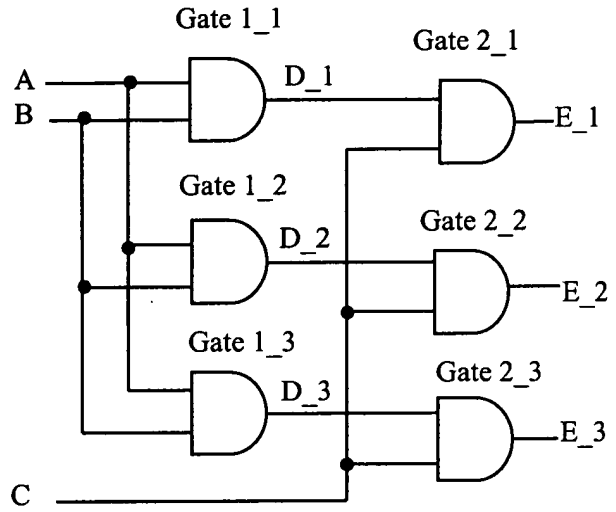


Fig. 6

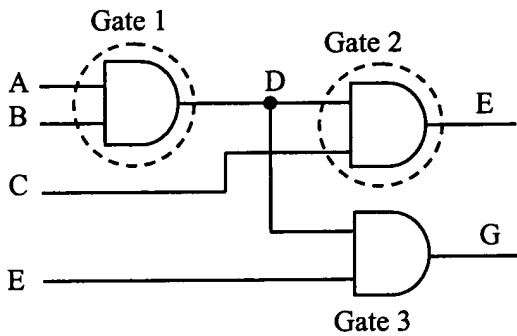
6A



6B



6C



6D

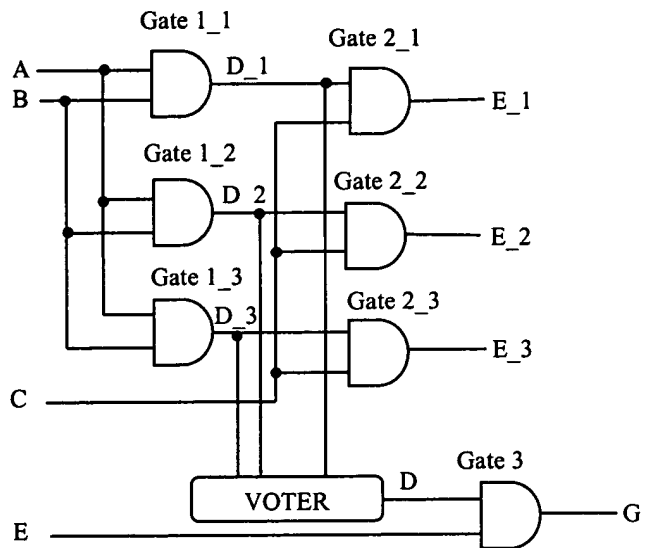


Fig. 7

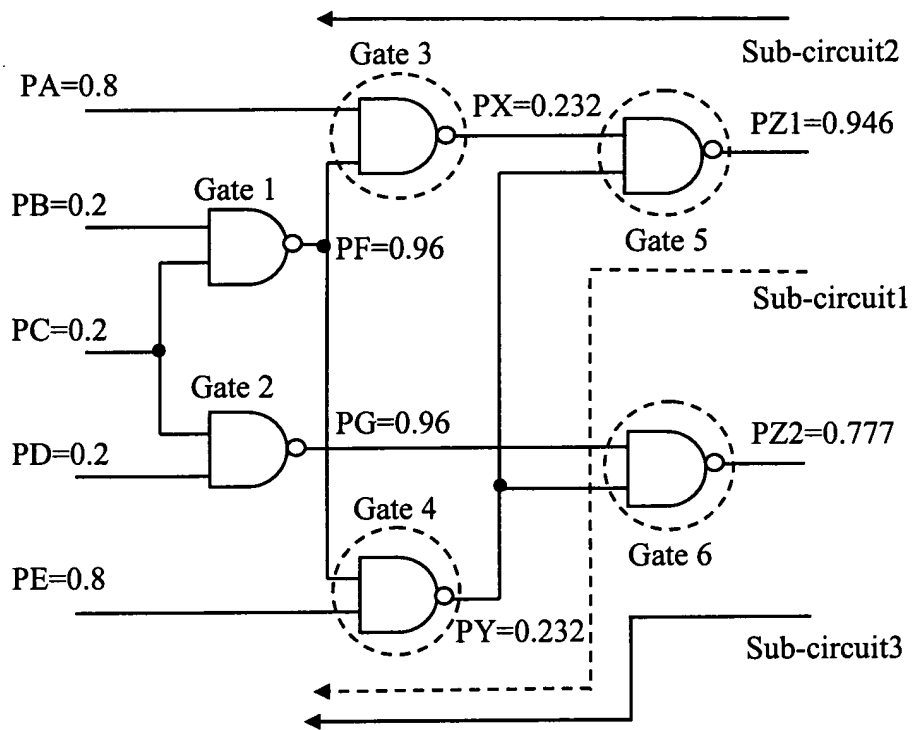


Fig. 8

